REMARKS

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising a first look-up-table, a second look-up-table and a logic circuit. The first look-up-table may be configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal. The second look-up-table may be configured to generate a second partial product signal from a second address formed by concatenating a third input signal and a fourth input signal. The logic circuit may be configure to generate an output signal in response to the first partial product signal and the second partial product signal. The first look-up-table and the second look-up-table may be implemented within a multiport memory.

SUPPORT FOR THE CLAIM AMENDMENTS

The amendments involve word deletions. Thus, no new matter has been added and no new issues have been raised.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 7-11 under 35 U.S.C. §112, second paragraph, is respectfully traversed and should be withdrawn.

Claim 7, through dependency on claim 1, provides (i) a first look-up-table configured to generate a first partial product signal from a first address formed by concatenating a first input signal and (ii) a second input signal and a second look-up-table configured to generate a second partial product signal from a second address formed by concatenating a third input signal and a fourth input signal. An example apparatus per claim 7 is shown in FIG. 1 of the application with four look-up tables 102a-n and four signals INa, INb, INc and INd. One of ordinary skill in the art would understand that the four input signals of the claim may be illustrated, for example, by the four signals INa, INb, INc and INd. Therefore, the claimed first and the second look-up tables may be illustrated by either (i) the LUT 102b and LUT 102c or (ii) the LUT 102n and LUT 102a. Using the example where the first claimed look-up-table is illustrated by the LUT 102b, the third claimed look-up-table may be illustrated by the LUT 102n with the claimed first and fourth input signals being illustrated by the signals INa and INc, respectively. Furthermore, the fourth claimed look-up-table (Claim 8) may be illustrated by the LUT 102a with the claimed second and third input signals being illustrated by the signals INd and INb, respectively. As such, claims 7 and 8 are fully compliant with 35 U.S.C. §112, second paragraph and the rejection should be withdrawn.

Claim 10 provides shifting a first partial product signal. Using the above example where the claimed first look-up-table is illustrated by the LUT 102b in FIG. 1 of the application, the claimed first partial product signal may be illustrated by the signal RESULTb generated from the signals INa and INd. The equation on page 8, line 3 of the application shows the partial product signal RESULTb for an example multiplication (e.g., ".") of A time D (e.g., A.D) that has been shifted (e.g., A.D0). The same multiplication and shift is also illustrated on page 7, lines 13-21 of the application. Therefore, claim 10 is fully compliant with 35 U.S.C. §112, second paragraph and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-11 and 13-20 under 35 U.S.C. §102(b) as being anticipated by White '151 is respectfully traversed and should be withdrawn.

White discloses a ROM-based complex multiplier useful for FFT butterfly arithmetic unit (Title). In contrast, the present invention concerns an apparatus comprising a first look-up-table, a second look-up-table and a logic circuit. The first look-up-table may be configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal. The second look-up-table may be

configured to generate a second partial product signal from a second address formed by concatenating a third input signal and a fourth input signal. The logic circuit may be configure to generate an output signal in response to the first partial product signal and the second partial product signal. The first look-up-table and the second look-up-table may be implemented within a multiport memory. White does not appear to disclose or suggest every element as arranged in the claims. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 1 provides a first look-up-table configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal. In contrast, White appears to be silent regarding any memory element 21-28 utilizing an address formed by concatenating two input signals. In particular, column 4, line 17 of White states that elements 15, 16, 17 and 18 are summing means for the addresses Ar, Br, Ai and Bi. A common definition for a "sum" is provided in Appendix A stating that a "sum is the result of an addition." However, Appendix B defines a "concatenation of two strings *a* and *b* [a]s the string *ab* formed by joining *a* and *b*." One of ordinary skill in the art using the common definitions provided in Appendices A and B would understand a summation to be a different operation than a concatenation. Therefore, White does not appear

to teach or suggest a first look-up table configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal as presently claimed.

Claim 1 further provides a multiport memory. The United States Patent and Trademark Office defines a multiport memory in class 711, subclass 149 as:

> Subject matter including means or steps for controlling **shared memory** capable of supporting a plurality of simultaneous read accesses. (Emphasis added)

One of ordinary skill in the art would not recognize the independent memory elements 21-28 of White, each having a single address input and a single data output, to form a shared memory of a conventional multiport memory. Therefore, White does not appear to disclose or suggest a multiport memory as presently claimed.

Claim 1 provides four input signals. In contrast, page 2, item 2, lines 3-7 of the Office Action only cites three address signals (Br, Ar and Ai) from White. Since three prior art signals cannot anticipate four claimed signals, a *prima facie* case of anticipation has not been established. Claims 14 and 15 use language similar to claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides that the multiport memory comprises a dual port memory. In contrast, White appears to be silent

regarding dual port memories. Therefore, White does not appear to disclose or suggest a multiport memory comprising a dual port memory as presently claimed. Furthermore, the Office Action does not appear to make any argument that dual port memories are expressly or inherently disclosed by White. Therefore, *prima facie* anticipation has not been established by the Office Action. As such, claim 2 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 3 provide that the multiport memory comprises a quad port memory. In contrast, White appears to be silent regarding quad port memories. Therefore, White does not appear to teach or suggest a multiport memory comprising a quad port memory as presently claimed. Assuming, *arguendo*, that the four address inputs shown in FIG. 1 of White constitutes a "quad port" (for which the Applicants' representative does not necessarily agree), (i) no memory elements 21-28 of White appear to be accessible by all four ports and (ii) no collection of memory elements 21-28 of White appear to form a shared memory per the US Patent and Trademark classification of a multiport memory. Therefore, the "quad ports" asserted by the Office Action do not appear to establish *prima facie* anticipation for a multiport memory comprising a quad port memory as presently claimed. As such, claim 3 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 5 provides a first input signal that is substantially equal to one of a third input signal and a fourth input signal. In contrast, White appears to be silent regarding using a substantially equal signal for two addresses into two of the memory elements 21-28. In particular, FIGS. 1-6 appear to disclose that the address received by each memory element 21-28 is unique. Furthermore, the assertion on page 2, item 2, line 11 of the Office Action to "note the above paragraph" does not appear to provide any evidence that White discloses or suggests substantially equal input signals. Nothing in the cited paragraph (page 2, item 2, lines 3-7 of the Office Action) appears to be a reference to substantially equal inputs. Therefore, White does not appear to disclose or suggest a first input signal that is substantially equal to one of a third input signal and a fourth input signal as presently claimed. As such, claim 5 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 6 provides a first input signal that comprises a single-bit serial configuration. In contrast, White appears to be silent regarding a single-bit serial configuration for the address inputs. Therefore, White does not appear to disclose or suggest a first input signal that comprises a single-bit serial configuration as presently claimed. Furthermore, the assertion on page 2, item 2, lines 11-12 of the Office Action that "if data is represented as a single bit then there is no difference between a serial and a

parallel configuration" does not appear to be expressly or inherently disclosed or suggested by White (see *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Circ. 1987)). Therefore, the "if" situation is irrelevant as White appears to be silent regarding the proposed single-bit parallel configuration. Claim 17 provides language similar to claim 6. As such, claims 6 and 17 are fully patentable over the cited reference and the rejection should be withdrawn.

Claims 7-11, 13 and 16-20 have been rejected under 35 U.S.C. §102(b) as being anticipated by White per page 2, item 2, lines 1-2 of the Office Action. However, no rational for the 102 rejection appears to be provided in the Office Action. Therefore, *prima facie* anticipation has not been established for lack of evidence that White expressly or inherently discloses or suggests every element as arranged in the claims (*Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984). As such, claims 7-11, 13 and 16-20 are fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 12 under 35 U.S.C. §103(a) as being unpatentable over White in view of Chehrazi et al. '843 is respectfully traversed and should be withdrawn.

The Office Action has failed to establish prima facie obviousness for lack of clear and particular evidence to combine the references. The Office Action fails to provide particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited references for combination. The factual inquiry whether to combine references must be thorough and searching. The rigorous application of the requirement for showing the teaching or motivation to combine references is necessary to avoid the subtle but powerful attraction of a hindsight-based obviousness analysis. It is improper, in determining whether a person of ordinary skill in the art would have been led to the combination of references, simply to use that which the inventor taught against its teacher. As such, because the Office Action fails to provide particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited references for combination, the Office Action does not appear to have met the Office's burden of factually establishing a *prima facie* case of obviousness (see MPEP §2142). Therefore, claim 12 is fully patentable over the cited references and the rejection should be withdrawn.

FINALITY OF THE OFFICE ACTION

Applicants' representative respectfully requests reconsideration of the finality of the July 3, 2003 Office Action. In particular, 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's action **will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

MPEP §706.07 further states:

> In making the final rejection, all outstanding ground of rejection of record should be carefully reviewed, and any such grounds relied on in the final rejection should be reiterated. **They must also be clearly developed to such an extent that applicant may readily judge the advisability of an appeal** unless a single previous Office action contains a complete statement supporting the rejection. (Emphasis added)

Regarding the 35 U.S.C. §112, second paragraph indefinite rejection, MPEP §2173.06 states:

> First, where the degree of uncertainty is not great, and where the claim is subject to more than one interpretation and at least one interpretation would render the claim unpatentable over the prior art, an appropriate course of action would be for the examiner to enter two rejections: (A) a rejection based on indefiniteness under 35 U.S.C. 112, second paragraph; **and (B) a rejection over the prior art** based on the interpretation of the claims which renders the prior art applicable. (Emphasis added)

The Office Action has failed to clearly developed the rejections for claims 1, 2, 6-11, 13-17 and 20 in sufficient detail for

Applicants to readily judge the advisability of an appeal. In particular, the Office Action does not argue anticipation for all of the elements as arranged in claims 1, 14 and 15. No rational appears to exist in the Office Action for rejecting claims 2, 13, 16 and 20 under 35 U.S.C. §102(b) based upon White. No rational appears to exist in the Office Action for rejecting claims 7-11 under 35 U.S.C. §102(b) based upon White per MPEP §2173.06. Furthermore, the arguments in the Office Action for claim 6 and 17 do not appear to be based on anything expressly or inherently disclosed or suggested by White. As such, the final rejections are premature and should be withdrawn.

The Examiner is respectfully requested to refrain from omnibus rejections that simply point to a single figure and assert that all of the claim elements are anticipated (see MPEP 707.07(d)). As such, Applicants' representative respectfully requests that subsequent rejections (if any) be presented in a non-final Office Action, to allow an opportunity to respond on the merits for all of the claims.

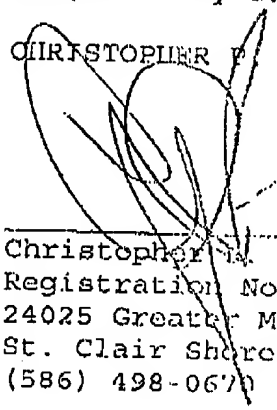
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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Dated: August 27, 2003

Docket No.:0325.00364

Appendix A

Sum

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A sum is the result of an addition. For example, adding 1, 2, 3, and 4 gives the sum 10, written

$$1 + 2 + 3 + 4 = 10. \tag{1}$$

The numbers being summed are called addends, or sometimes summands. The summation operation can also be indicated using a capital sigma with upper and lower limits written above and below, and the index indicated below. For example, the above sum could be written

$$\sum_{k=1}^{4} k = 10. \tag{2}$$

The sum of a list of numbers is implemented as `Total[list]` in *Mathematica* version 5.0.

A sum

$$\sum_{k=1}^{n} a_k \tag{3}$$

in which each term a_i is given by some fixed rule (i.e., $\{a_i\}_{i=1}^{n}$ is a well defined sequence) is called a series, and if the number of terms n is infinite, the sum is called an infinite series. A sum of the form

$$\sum_{k=1}^{n} r^k \tag{4}$$

is called a geometric series.

The general finite power sum

http://mathworld.wolfram.com/Sum.html

Appendix A

$$\sum_{k=1}^{n} k^p \tag{5}$$

can be given by the expression

$$\sum_{k=1}^{n} k^p = \frac{(B+n+1)^{[p+1]} - B^{[p+1]}}{p+1}, \tag{6}$$

which is equivalent to Faulhaber's formula, where the notation $B^{[k]}$ means the quantity in question is raised to the appropriate power k and all terms of the form B^m are replaced with the corresponding Bernoulli numbers B_m.

An amusing identity due to J. Ziegenbein (pers. comm., June 19, 2002) follows from the identity

$$n^2 - \tfrac{1}{2}(n-1)n = \tfrac{1}{2}n(n+1), \tag{7}$$

which can be written

$$n^2 - \sum_{k=1}^{n-1} k = \sum_{k=1}^{n} k. \tag{8}$$

Therefore, $\sum_{k=1}^{10} k = 55$, for example, can be written in the equivalent forms

$$\sum_{k=1}^{10} k = 10^2 - \left(\sum_{k=1}^{9} k\right) \tag{9}$$

$$= 10^2 - \left(9^2 - \left(\sum_{k=1}^{8} k\right)\right) \tag{10}$$

$$= 10^2 - \left(9^2 - \left(8^2 - \left(\sum_{k=1}^{7} k\right)\right)\right) \tag{11}$$

$$= 10^2 - \left(9^2 - \left(8^2 - \left(7^2 - \left(\sum_{k=1}^{6} k\right)\right)\right)\right) \tag{12}$$

and so on.

Nicomachus's theorem gives as curious expression for the power sum $\sum_{k=1}^{n} k^3$.

Special sums include

$$\sum_{j=1}^{n} \frac{x_j^r}{\prod_{\substack{k=1 \\ k\neq j}}^{n}(x_j - x_k)} = \begin{cases} 0 & \text{for } 0 \leq r < n-1 \\ 1 & \text{for } r = n-1 \\ \sum_{j=1}^{n} x_j & \text{for } r = n \end{cases} \tag{13}$$

and

$$\sum_{k=1}^{n} \frac{\prod_{r=1, r\neq k}^{n}(x + k - r)}{\prod_{r=1, r\neq k}^{n}(k - r)} = 1 \tag{14}$$

To minimize the sum of a set of squares of numbers $\{x_i\}$ about a given number x_0

$$S \equiv \sum_i (x_i - x_0)^2 = \sum_i x_i^2 - 2x_0 \sum_i x_i + N x_0^2, \tag{15}$$

take the derivative,

$$\frac{d}{dx_0} S = -2 \sum_i x_i + 2N x_0 = 0. \tag{16}$$

Solving for x_0 gives

$$x_0 \equiv \bar{x} = \frac{1}{N} \sum_i x_i, \tag{17}$$

so S is minimized when x_0 is set to the mean.

SEE ALSO Arithmetic Series, Bernoulli Number, Binomial Sums, Clark's Triangle, Convergence Improvement, Dedekind Sum, Double Series, Euler Sum, Factorial Sums, Faulhaber's Formula, Gabriel's Staircase, Gaussian Sum, Geometric Series, Gosper's Method, Hurwitz Zeta Function, Infinite Series, Infinite Product, Kloosterman's Sum, Legendre Sum, Lerch Transcendent, Nicomachus's Theorem, Odd Number Theorem, Pascal's Triangle, Power Sum, Product,

Appendix B

Ramanujan's Sum, Riemann Zeta Function, Series, Whitney Sum

References

Courant, R. and Robbins, H. "The Sum of the First n Squares." §1.4 in *What Is Mathematics?: An Elementary Approach to Ideas and Methods, 2nd ed.* Oxford, England: Oxford University Press, pp. 14-15, 1996.

Petkovsek, M.; Wilf, H. S.; and Zeilberger, D. *A = B*. Wellesley, MA: A. K. Peters, 1996.

Eric W. Weisstein

Appendix B

Concatenation

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The concatenation of two strings a and b is the string ab formed by joining a and b. Thus the concatenation of the strings "book" and "ease" is the string "bookcase". The concatenation of two strings a and b is often denoted ab, $a||b$, or, in *Mathematica*, $a <> b$.

Concatenation is an associative operation, so that the concatenation of three or more strings, for example abc, $abcd$, etc., is well defined.

The concatenation of two or more numbers is the number formed by concatenating their numerals. For example, the concatenation of 1, 234, and 5678 is 12345678. The value of the result depends on the numeric base, which is typically understood from context.

The formula for the concatenation of numbers p and q in base b is

$$p||q = pb^{l(q)} + q,$$

where

$$l(q) = \lfloor \log_b q \rfloor + 1$$

is the number length of q in base b and $\lfloor x \rfloor$ is the floor function.

SEE ALSO Consecutive Number Sequences, Number Length, Smarandache Sequences

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